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[Title Of The Invention]
SEMICONDUCTOR DEVICE

[Abstract]
PROBLEM TO BE SOLVED: To make it possible to make low a lead inductance in a semiconductor device and to obtain a large capacitance by a method wherein the first terminal of a second planar conductor and a ground terminal are connected with each other.
SOLUTION: A first terminal 31-1 of a second planar conductor 31 and a ground terminal 29 are connected with each other via a wiring pattern 35 and bonding pads 26-1 for signal input/output use on an IC die 26 are connected with signal input/output terminals 27 through a wiring pattern 35 which is provided on a substrate 25. A dielectric material 32 is held between planar conductors 30 and 31, is superposed on the conductor 31 to constitute a capacitor and at the same time, a power current is made to flow through the conductor 30 going through a first terminal 30-1 of a first planar conductor from a power terminal 28. A return current is made to flow through the conductor 31 going through a second terminal 31-2 of the conductor 31 from a bonding pad 26-3 for grounding use of the die 26. Moreover, as the return current is made to flow to the terminal 29 via the terminal 31-1 of the conductor 31, the capacitor provides a distributed capacitance to a current path and noise can be passed in a wide band.

[Claim(s)]
[Claim 1]A substrate which has two or more signal input/output terminals, at least one power supply terminal, and at least one earthing terminal, At least one IC die which has two or more bonding pads for signal input and output and at least one bonding pad for power supplies which were connected to a circuit pattern which surface mounting was carried out to this substrate, and was provided in the above-mentioned substrate, respectively, and at least one bonding pad for grounding, It has a capacitor which was formed on both sides of a dielectric with the first and the second surface state conductor, and was allocated by the above-mentioned substrate, Said first and the second surface state conductor provide second at least one terminal in one end of surface state at first at least one terminal and the other end of surface state, Connect said power supply terminal and the first terminal of said first surface state conductor, and each bonding pad for power supplies of said IC die is connected with the second terminal of this first surface state conductor, A semiconductor device which connected the second terminal of said second surface state conductor with each bonding pad for grounding of said IC die, and connected this the second terminal and said earthing terminal of a surface state conductor. [first]
[Claim 2]At least one IC die by which a bonding pad was connected to an allocation pattern which surface mounting was carried out to one field of a substrate provided with two or more through holes which flow through substrate both sides, and this board, and was provided in the above-mentioned substrate, respectively, Two or more signal input/output terminals and at least one power supply terminal which were provided in a

field of another side of this board, and at least one earthing terminal, It is allocated in free space of this terminal and the above-mentioned substrate except a through hole, and has a capacitor formed on both sides of a dielectric with the first and the second surface state conductor, The first and the second surface state conductor provide second at least one terminal in one end of surface state at first at least one terminal and the other end of surface state, A power supply terminal provided in this substrate is connected with the first terminal of the first surface state conductor, A through hole established in the first terminal and said substrate of a surface state conductor is connected, [second] A circuit pattern linked to a bonding pad for power supplies of this through hole and said IC die is connected, A semiconductor device which connected a circuit pattern which connects with the first terminal of the second surface state conductor an earthing terminal formed in this substrate, connects a through hole established in the second terminal and said substrate of a surface state conductor, and is connected to a bonding pad for grounding of this through hole and said IC die. [second]

[Claim 3]On both sides of a dielectric, it is formed in one field of a substrate provided with two or more through holes which flow through substrate both sides, and this substrate in free space except said through hole with the first and the second surface state conductor, A capacitor which provided second at least one terminal in one end of surface state of the first and the second surface state conductor at first at least one terminal and the other end of surface state, Two or more signal input/output terminals and at least one power supply terminal which were provided in a field of another side of this board, and at least one earthing terminal, It is mounted in a field of another side of the above-mentioned substrate, and has at least one IC die connected to a circuit pattern formed in a field of another side of the above-mentioned substrate, A power supply terminal provided in this substrate is connected with the first terminal of the first surface state conductor of said capacitor via a through hole established in said substrate, The second terminal of the first surface state conductor is connected with a circuit pattern connected to a bonding pad for power supplies of said IC die via other through holes established in said substrate, An earthing terminal formed in this substrate is connected with the first terminal of the second surface state conductor of said capacitor via a through hole established in said substrate, A semiconductor device linked to a circuit pattern which connects the second terminal of the second surface state conductor to a bonding pad for grounding of said IC die via other through holes established in said substrate.

[Claim 4]The semiconductor device according to any one of claims 1 to 3 having arranged each of a signal input/output terminal, a power supply terminal, and an earthing terminal which were formed in a substrate in the shape of a lattice by a spherical shape.

[Claim 5]The semiconductor device according to any one of claims 1 to 3 having arranged each of a signal input/output terminal, a power supply terminal, and an earthing terminal which were formed in a substrate in the shape of a lattice with pin geometry.

[Claim 6]The semiconductor device according to any one of claims 1 to 3 forming a capacitor in a substrate by printing.

[Claim 7]It has a TAB package characterized by comprising the following which mounted an IC die in at least one carrier film, The first power supply terminal provided in this carrier film is connected with the second power supply terminal, connecting the second power supply terminal with the first terminal of said second surface state conductor -- this -- it connecting with the third power supply terminal of a carrier film, and the second

terminal of the second surface state conductor, The third power supply terminal is connected to a bonding pad for power supplies of said IC die, The first earthing terminal formed in this carrier film is connected with the second earthing terminal, connecting the second earthing terminal with the first terminal of said second surface state conductor -- this -- it connecting with the third earthing terminal of a carrier film, and the second terminal of the second surface state conductor, A semiconductor device which connected the third earthing terminal to a bonding pad for grounding of said IC die, connected with the second signal input/output terminal the first signal input/output terminal provided in this carrier film, and connected the second signal input/output terminal to a bonding pad for signal input and output of said IC die.

A substrate.

A capacitor which it was allocated on this substrate and formed in one end of surface state on both sides of a dielectric with first at least one terminal, the first which has second at least one terminal in the other end of surface state, and the second surface state conductor. It is arranged in piles on this capacitor, Two or more first signal input/output terminals. It has two or more second signal input/output terminals, first at least one power supply terminal, first at least one earthing terminal, second at least one power supply terminal, second at least one earthing terminal, third at least one power supply terminal, and third at least one earthing terminal, Two or more bonding pads for signal input and output, at least one bonding pad for power supplies, and at least one bonding pad for grounding.

[Claim 8]The semiconductor device according to claim 7 which made plate shape each of the first signal input/output terminal, the first power supply terminal, and the second earthing terminal.

[Claim 9]The semiconductor device according to claim 7 which has arranged each of the first signal input/output terminal, the first power supply terminal, and the first earthing terminal in the shape of a lattice by a spherical shape.

[Claim 10]The semiconductor device according to claim 7 which has arranged each of the first signal input/output terminal, the first power supply terminal, and the first earthing terminal in the shape of a lattice with pin geometry.

[Claim 11]It has a TAB package characterized by comprising the following which mounted an IC die in at least one carrier film, The first power supply terminal provided in this carrier film is connected with the second power supply terminal, connecting the second power supply terminal with the first terminal of said second surface state conductor -- this -- it connecting with the third power supply terminal of a carrier film, and the second terminal of the second surface state conductor, The third power supply terminal is connected to a bonding pad for power supplies of said IC die, The first earthing terminal formed in this carrier film is connected with the second earthing terminal, connecting the second earthing terminal with the first terminal of said second surface state conductor -- this -- it connecting with the third earthing terminal of a carrier film, and the second terminal of the second surface state conductor, The third earthing terminal is connected to a bonding pad for grounding of said IC die, A semiconductor device which connected with the second signal input/output terminal the first signal input/output terminal provided in this carrier film, connected the second signal input/output terminal to a bonding pad for signal input and output of said IC die, and has been arranged on both sides of said capacitor with said back up plate and said TAB package.

A substrate reinforced by the back up plate.

A capacitor which it was allocated on this substrate and formed in one end of surface state on both sides of a dielectric with first at least one terminal, the first which has second at least one terminal in the other end of surface state, and the second surface state conductor. It is arranged in piles on this capacitor, Two or more first signal input/output terminals. It has two or more second signal input/output terminals, first at least one power supply terminal, first at least one earthing terminal, second at least one power supply terminal, second at least one earthing terminal, third at least one power supply terminal, and third at least one earthing terminal, Two or more bonding pads for signal input and output, at least one bonding pad for power supplies, and at least one bonding pad for grounding.
[Claim 12]The semiconductor device according to claim 11 which used the back up plate as metal.
[Claim 13]The semiconductor device according to claim 11 which carried out alumite treatment of the surface of this aluminum while making the back up plate into aluminum.
[Claim 14]The semiconductor device according to claim 11 which formed a capacitor in the back up plate by printing.

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to the semiconductor device having capacitors, such as a microprocessor which carries out high-speed operation.
[0002]
[Description of the Prior Art]Drawing 6 is a perspective view of the conventional pin grid array form ceramic package for high-speed microprocessors. In drawing 6, 1 is a terminal, 2 is the package base which arranged the terminal 1 in the shape of a lattice, 3 is a laminated ceramic capacitor (it is henceforth called a chip capacitor) of a surface mounting type, and 4 is a radiator. Although not illustrated by drawing 6, it is built in the package base 2, and is connected to the terminal 1 arranged in the shape of a lattice, and the die of a microprocessor has cooled generation of heat at the time of operation with the radiator 4.
[0003]The terminal of the two poles of the chip capacitor 3 mounted in the package base 2 is connected also to the terminal 1 while being connected to at least one power supply terminal and earthing terminal of a microprocessor, respectively.
[0004]Drawing 7 is a sectional view of the semiconductor device in which the capacitor was formed on the IC die given in JP,63-239970,A. In drawing 7, 5 is a die of IC, 6 is a circuit formation side of IC, 7 is the power supply wiring inside a die, and 8 is the grounding wiring inside a die. 9 and 10 are polyimide system resin layers, 11, 12, and 13 are through holes, 14 and 15 are electrode metal layers, 16 is a metal layer, and 17, 18, and 19 are terminal areas. It is what formed the capacitor which the electrode metal layers 14 and 15 were made to counter via the polyimide system resin layer 10 on the circuit formation side 6 of IC via the polyimide system resin layer 9, The electrode metal layer 14 is the capacitor of a concentrated-constant form which connected the electrode metal layer 15 to the internal power supply wiring 7 via the terminal areas 18 and 19 at the grounding wiring 8 inside a die via the terminal area 17, respectively.
[0005]
[Problem(s) to be Solved by the Invention]In order to accelerate a computer, while accelerating a bus clock, internal clock frequency of a microprocessor is usually made high. In this case, the power consumption of the microprocessor increased and it had a

problem of a high frequency noise being overlapped on power supply voltage, and making a microprocessor malfunction by the load change by the bus clock and lenience-and-severity operation which a microprocessor is not only overheated, but were accelerated.
[0006]In the case of the circuit which uses the bypass capacitor of the conventional concentrated-constant type shown in drawing 6 and drawing 7. The very small amplitude current which absorbs the high frequency ripple capacity of a capacitor is small, and the terminal of lead inductance of a capacitor is very small at the electrode for soldering for surface mounting, and according to a high frequency noise only flows. Therefore, to the load change of a lenience and severity microprocessor, several kinds of capacitors of low equivalent series resistance must be prepared, arrangement connection must be made near a power supply terminal and the earthing terminal, and a load change must be buffered according to the discharge current.
[0007]In the case of the conventional pin grid array form ceramic package for high-speed microprocessors of drawing 6, the use which connects the bypass capacitor of many concentrated-constants type to the electrode terminal pads and the earthing terminal pad of a large number in which it was provided by the die, and absorbs the high frequency ripple by a high frequency noise is presented.
[0008]Thus, in the semiconductor device which constituted the conventional capacitor, to the load change of a lenience and severity microprocessor, multiple connection of the bypass capacitor of further the concentrated-constant type of various sorts must be carried out, and the package base of a large area must be prepared, or it must mount out of a package. In this case, while wiring impedance increased and the buffer effect of the load change decreased, there was a problem which requires a complicated mounting man day.
[0009]This invention solves such a conventional problem.
The purpose is to provide the semiconductor device which lead inductance can be made low, and large electric capacity is obtained, and can absorb the noise of a broadband.
[0010]
[Means for Solving the Problem]In order to solve the above-mentioned technical problem, a semiconductor device of this invention, Form a capacitor in a substrate with which an IC die was mounted, and one side of this capacitor electrode is considered as wiring which connects between a power supply terminal of a die, and earthing terminals, Another side of a capacitor electrode is considered as wiring which connects between an earthing terminal of a die, and earthing terminals, and power supply current is made to flow into a power supply terminal of a die via one side of a capacitor electrode from a power supply terminal of a device, and it is made to flow out of an earthing terminal of a die into an earthing terminal of a device via another side of a capacitor electrode. Therefore, it can carry out [large scale]-izing in a broad electrode while it can make lead inductance to a die low, since this capacitor considers a broad electrode as connection wiring, and it has composition which allotted distributed capacity to a current path.
[0011]A noise of a broadband is absorbable in a mass field integrated by this composition from a small capacity field over which it was distributed.
[0012]
[Embodiment of the Invention]The substrate with which the invention of this invention according to claim 1 has two or more signal input/output terminals, at least one power supply terminal, and at least one earthing terminal, At least one IC die which has two or more bonding pads for signal input and output and at least one bonding pad for power

supplies which were connected to the circuit pattern which surface mounting was carried out to this substrate, and was provided in the above-mentioned substrate, respectively, and at least one bonding pad for grounding, It has the capacitor which was formed on both sides of the dielectric with the first and the second surface state conductor, and was allocated by the above-mentioned substrate, Said first and the second surface state conductor provide second at least one terminal in one end of surface state at first at least one terminal and the other end of surface state, Connect said power supply terminal and the first terminal of said first surface state conductor, and each bonding pad for power supplies of said IC die is connected with the second terminal of this first surface state conductor, The second terminal of said second surface state conductor is connected with each bonding pad for grounding of said IC die, Are the semiconductor device which connected this the second terminal and said earthing terminal of the surface state conductor, constitute a capacitor from piling up on both sides of a dielectric with a surface state conductor, and power supply current is sent through a surface state conductor via the first terminal of the first surface state conductor from a power supply terminal, [first] While passing to the bonding pad for power supplies of an IC die via the second terminal of the first [further] surface state conductor, It can be made to function as a capacitor which allots distributed capacity to the current path which sends return currents through a surface state conductor via the second terminal of the second surface state conductor from the bonding pad for grounding of an IC die, and also was poured to the earthing terminal via the first terminal of the second surface state conductor. Having, the high frequency component of the broadband noise superimposed on power supply voltage is a low capacity region near a power supply terminal, and an inside low-frequency component has the operation of making it bypass in the mass region of a up to [from a power supply terminal] near the IC die.

[0013]The substrate provided with two or more through holes where the invention of this invention according to claim 2 flows through substrate both sides, At least one IC die by which the bonding pad was connected to the circuit pattern which surface mounting was carried out to one field of this board, and was provided in the above-mentioned substrate, respectively, Two or more signal input/output terminals and at least one power supply terminal which were provided in the field of another side of this board, and at least one earthing terminal, It is allocated in the free space of this terminal and the above-mentioned substrate except a through hole, and has the capacitor formed on both sides of the dielectric with the first and the second surface state conductor, The first and the second surface state conductor provide second at least one terminal in one end of surface state at first at least one terminal and the other end of surface state, The power supply terminal provided in this substrate is connected with the first terminal of the first surface state conductor, The through hole established in the first terminal and said substrate of the surface state conductor is connected, [second] The circuit pattern linked to the bonding pad for power supplies of this through hole and said IC die is connected, It is the semiconductor device which connected the circuit pattern which connects with the first terminal of the second surface state conductor the earthing terminal formed in this substrate, connects the through hole established in the second terminal and said substrate of the surface state conductor, and is connected to the bonding pad for grounding of this through hole and said IC die, [second] The operation of carrying out noise absorption rather than claim 1 in a broadband is carried out.

[0014]The substrate provided with two or more through holes where the invention of this invention according to claim 3 flows through substrate both sides, On both sides of a dielectric, it is formed in one field of this substrate in the free space except said through hole with the first and the second surface state conductor, The capacitor which provided second at least one terminal in one end of the surface state of the first and the second surface state conductor at first at least one terminal and the other end of surface state, Two or more signal input/output terminals and at least one power supply terminal which were provided in the field of another side of this board, and at least one earthing terminal, It is mounted in the field of another side of the above-mentioned substrate, and has at least one IC die connected to the circuit pattern formed in the field of another side of the above-mentioned substrate, The power supply terminal provided in this substrate is connected with the first terminal of the first surface state conductor of said capacitor via the through hole established in said substrate, The second terminal of the first surface state conductor is connected with the circuit pattern connected to the bonding pad for power supplies of said IC die via other through holes established in said substrate, The earthing terminal formed in this substrate is connected with the first terminal of the second surface state conductor of said capacitor via the through hole established in said substrate, The second terminal of the second surface state conductor is a semiconductor device linked to the circuit pattern connected to the bonding pad for grounding of said IC die via other through holes established in said substrate, and carries out the operation of carrying out noise absorption rather than claim 2 in a broadband.

[0015]By a spherical shape, the signal input/output terminal, power supply terminal, and earthing terminal which the invention of this invention according to claim 4 formed in the substrate in the semiconductor device according to any one of claims 1 to 3 are arranged in the shape of a lattice, and have the operation of making surface mounting possible, respectively.

[0016]With pin geometry, the signal input/output terminal, power supply terminal, and earthing terminal which the invention of this invention according to claim 5 formed in the substrate in the semiconductor device according to any one of claims 1 to 3 are arranged in the shape of a lattice, and have the operation of enabling socket mounting, respectively.

[0017]In the semiconductor device according to any one of claims 1 to 3, the invention of this invention according to claim 6 forms a capacitor in a substrate by printing, and has the operation of excelling in productive efficiency.

[0018]The invention of this invention according to claim 7 is allocated on a substrate and this substrate, The capacitor formed in one end of surface state on both sides of the dielectric with first at least one terminal, the first which has second at least one terminal in the other end of surface state, and the second surface state conductor, It is arranged in piles on this capacitor, Two or more first signal input/output terminals. It has two or more second signal input/output terminals, first at least one power supply terminal, first at least one earthing terminal, second at least one power supply terminal, second at least one earthing terminal, third at least one power supply terminal, and third at least one earthing terminal, It has the TAB package which mounted the IC die which has two or more bonding pads for signal input and output, at least one bonding pad for power supplies, and at least one bonding pad for grounding in at least one carrier film, The first power supply terminal provided in this carrier film is connected with the second power supply terminal, connecting the second power supply terminal with the first terminal of said second surface

state conductor -- this -- the second terminal of the second surface state conductor being connected with the third power supply terminal of a carrier film, and the third power supply terminal being connected to the bonding pad for power supplies of said IC die, and, The first earthing terminal formed in this carrier film is connected with the second earthing terminal, connecting the second earthing terminal with the first terminal of said second surface state conductor -- this -- it connecting with the third earthing terminal of a carrier film, and the second terminal of the second surface state conductor, The third earthing terminal is connected to the bonding pad for grounding of said IC die, The first signal input/output terminal provided in this carrier film is connected with the second signal input/output terminal, the second signal input/output terminal is connected to the bonding pad for signal input and output of said IC die, and it has the operation that the zone of signal wiring is large.

[0019]In the semiconductor device according to claim 7, the invention of this invention according to claim 8 makes plate shape the first signal input/output terminal, first power supply terminal, and second earthing terminal, respectively, and has the operation of making surface mounting possible.

[0020]In the semiconductor device according to claim 7, the invention of this invention according to claim 9 arranges the first signal input/output terminal, first power supply terminal, and first earthing terminal in the shape of a lattice by a spherical shape, respectively, and has the operation of making Ogata surface mounting possible.

[0021]In the semiconductor device according to claim 7, the first signal input/output terminal, first power supply terminal, and first earthing terminal arrange each in the shape of a lattice with pin geometry, and the invention of this invention according to claim 10 has the operation of enabling socket mounting.

[0022]The substrate with which the invention of this invention according to claim 11 was reinforced by the back up plate, The capacitor which it was allocated on this substrate and formed in one end of surface state on both sides of the dielectric with first at least one terminal, the first which has second at least one terminal in the other end of surface state, and the second surface state conductor, It is arranged in piles on this capacitor, Two or more first signal input/output terminals. It has two or more second signal input/output terminals, first at least one power supply terminal, first at least one earthing terminal, second at least one power supply terminal, second at least one earthing terminal, third at least one power supply terminal, and third at least one earthing terminal, It has the TAB package which mounted the IC die which has two or more bonding pads for signal input and output, at least one bonding pad for power supplies, and at least one bonding pad for grounding in at least one carrier film, The first power supply terminal provided in this carrier film is connected with the second power supply terminal, connecting the second power supply terminal with the first terminal of said second surface state conductor -- this -- the second terminal of the second surface state conductor being connected with the third power supply terminal of a carrier film, and the third power supply terminal being connected to the bonding pad for power supplies of said IC die, and, The first earthing terminal formed in this carrier film is connected with the second earthing terminal, connecting the second earthing terminal with the first terminal of said second surface state conductor -- this -- it connecting with the third earthing terminal of a carrier film, and the second terminal of the second surface state conductor, The third earthing terminal is connected to the bonding pad for grounding of said IC die, The first signal input/output

terminal provided in this carrier film is connected with the second signal input/output terminal, The second signal input/output terminal is connected to the bonding pad for signal input and output of said IC die, and it arranges on both sides of said capacitor with the back up plate and said TAB package, and has the operation that shape is stable.
[0023]In the semiconductor device according to claim 11, the invention of this invention according to claim 12 uses the back up plate as metal, and has the operation of excelling in heat dissipation nature.
[0024]In the semiconductor device according to claim 11, the invention of this invention according to claim 13 carries out alumite treatment of the surface of this aluminum, and has the operation of excelling in heat dissipation nature while it makes the back up plate aluminum.
[0025]In the semiconductor device according to claim 11, the invention of this invention according to claim 14 prints and forms a capacitor in the back up plate, and has the operation of excelling in productive efficiency.
[0026]Drawing 1 is a sectional view of the pin grid array form package by a 1st embodiment of this invention. In drawing 1, 25 is a substrate, 26 is an IC die, and 27 is a signal input/output terminal (in this embodiment, for convenience). it is called a signal input/output terminal including a signal input terminal, a signal output terminal, and a signal input/output terminal -- it is -- 28 is a power supply terminal, 29 is an earthing terminal and the terminals 27, 28, and 29 are carrying out pin geometry, respectively. 30 is the first surface state conductor, 31 is the second surface state conductor, and 32 is a dielectric and constitutes the capacitor. 33 is a vamp, 34 is an insulating layer, and 35 is a circuit pattern. IC die 26 Many bonding pads 26-1 for signal input and output, It has at least one bonding pad 26-2 for power supplies, and at least one bonding pad 26-3 for grounding, and in drawing 1, after the vamp 33 is formed in each bonding pad, face down bonding is carried out to the substrate 25.
[0027]It is formed on the insulating layer 34 which covered and formed the circuit pattern 35 which formed the capacitor on both sides of the dielectric 32 with the first surface state conductor 30 and the second surface state conductor 31, and was formed in the component side of IC die 26 of the substrate 25.
[0028]The first surface state conductor 30 equips one end of surface state with second at least one terminal 30-2 at first at least one terminal 30-1 and the other end of surface state, The second surface state conductor 31 equips one end of surface state with second at least one terminal 31-2 at first at least one terminal 31-1 and the other end of surface state, The power supply terminal 28 and the first terminal 30-1 of the first surface state conductor 30 the second terminal 30-2 of the first surface state conductor, and each bonding pad 26-2 for power supplies of said IC die 26, The second terminal 31-2 of each bonding pad 26-3 for grounding of IC die 26, and the second surface state conductor 31, The second terminal 31-1 and said earthing terminal 29 of the surface state conductor 31 are connected via the circuit pattern 35, respectively, and the bonding pad 26-1 for signal input and output of IC die 26 is connected to the signal input/output terminal 27 by the circuit pattern 35 provided in the substrate 25. [first]
[0029]Thus, while constituting the capacitor piled with the surface state conductors 30 and 31 on both sides of the dielectric 32, Power supply current flows through the surface state conductor 30 via the first terminal 30-1 of the first surface state conductor from the power supply terminal 28, and also flows into the bonding pad 26-2 for power supplies of an IC

die via the second terminal 30-2 of the first surface state conductor.
[0030]Return currents flow through the surface state conductor 31 via the second terminal 31-2 of the second surface state conductor from the bonding pad 26-3 for grounding of an IC die, Since it flows into the earthing terminal 29 via the first terminal 31-1 of the second [further] surface state conductor, this capacitor is arranged for distributed capacity.
[0031]Therefore, the high frequency component of the broadband noise superimposed on power supply voltage is a low capacity region near the power supply terminal, and an inside low-frequency component can be made to bypass in the mass region of a up to [from a power supply terminal] near the IC die.
[0032]Drawing 2 is a sectional view of the pin grid array form package by a 2nd embodiment of this invention. In drawing 2, 26 is an IC die, 27 is a signal input/output terminal, 28 is a power supply terminal, 25 is a substrate and the terminals 27, 28, and 29 are carrying out [29 is an earthing terminal and] pin geometry. 30 is the first surface state conductor, 31 is the second surface state conductor, and 32 is a dielectric and constitutes the capacitor. 33 is a vamp, 35 is a circuit pattern, and 36 is a through hole.
[0033]IC die 26 Many bonding pads 26-1 for signal input and output, It has at least one bonding pad 26-2 for power supplies, and at least one bonding pad 26-3 for grounding, and in drawing 2, after the vamp 33 is formed in each bonding pad, face down bonding is carried out to the substrate 25.
[0034]It forms in the rear face of the circuit pattern 35 which formed the capacitor on both sides of the dielectric 32 with the first surface state conductor 30 and the second surface state conductor 31, and was formed in the substrate 25, and the field which mounted IC die 26.
[0035]The first surface state conductor 30 equips one end of surface state with second at least one terminal 30-2 at first at least one terminal 30-1 and the other end of surface state, The second surface state conductor 31 equips one end of surface state with second at least one terminal 31-2 at first at least one terminal 31-1 and the other end of surface state, The power supply terminal 28 and the first terminal 30-1 of the first surface state conductor 30 are connected via the through hole 36-1 and the circuit pattern 35, The second terminal 30-2 of the first surface state conductor and each bonding pad 26-2 for power supplies of said IC die 26 are connected via the through hole 36-2 and the circuit pattern 35, The second terminal 31-2 of each bonding pad 26-3 for grounding of IC die 26 and the second surface state conductor 31 is connected via the through hole 36-4 and the circuit pattern 35, The second terminal 31-1 and said earthing terminal 29 of the surface state conductor 31 are connected via the through hole 36-3 and the circuit pattern 35, and the bonding pad 26-1 for signal input and output of IC die 26 is connected to the signal input/output terminal 27 by the circuit pattern 35 provided in the substrate 25. [first]
[0036]Thus, while constituting the capacitor on which the dielectric 32 was piled up on both sides of the surface state conductors 30 and 31 like drawing 1, Power supply current flows through the surface state conductor 30 via the first terminal 30-1 of the first surface state conductor from the power supply terminal 28, and also flows into the bonding pad 26-2 for power supplies of an IC die via the second terminal 30-2 of the first surface state conductor.
[0037]Big electric capacity is obtained by forming this capacitor in the rear face of the substrate of IC die 26 and the terminal clamp face, and the difference with a first embodiment can absorb the noise of a broadband more.

[0038]Drawing 3 is a sectional view of the ball grid array form package by a 3rd embodiment of this invention. In drawing 3, 26 is an IC die, 27 is a signal input/output terminal, 28 is a power supply terminal, 25 is a substrate and the terminals 27, 28, and 29 are carrying out [29 is an earthing terminal and] the spherical shape, respectively. 30 is the first surface state dielectric, 31 is the second surface state conductor, and 32 is a dielectric and constitutes a capacitor. 33 is a vamp, 35 is a circuit pattern, and 36 is a through hole.

[0039]IC die 26 Many bonding pads 26-1 for signal input and output, It has at least one bonding pad 26-2 for power supplies, and at least one bonding pad 26-3 for grounding, and in drawing 3, after the vamp 33 is formed in each bonding pad, face down bonding is carried out to the substrate 25.

[0040]It forms in the rear face of the circuit pattern 35 which formed the capacitor on both sides of the dielectric 32 with the first surface state conductor 30 and the second surface state conductor 31, and was formed in the substrate 25, and the field which mounted IC die 26.

[0041]The first surface state conductor 30 equips one end of surface state with second at least one terminal 30-2 at first at least one terminal 30-1 and the other end of surface state, The second surface state conductor 31 equips one end of surface state with second at least one terminal 31-2 at first at least one terminal 31-1 and the other end of surface state, The power supply terminal 28 and the first terminal 30-1 of the first surface state conductor 30 are connected, The second terminal 30-2 of the first surface state conductor and each bonding pad 26-2 for power supplies of said IC die 26 are connected via the through hole 36-2 and the circuit pattern 35, The second terminal 31-2 of each bonding pad 26-3 for grounding of IC die 26 and the second surface state conductor 31 is connected via the through hole 36-4 and the circuit pattern 35, The second terminal 31-1 and said earthing terminal 29 of the surface state conductor 31 are connected, and the bonding pad 26-1 for signal input and output of IC die 26 is connected to the signal input/output terminal 27 via the circuit pattern 35 and the through hole 36-5 which were established in the substrate 25. [first]

[0042]Thus, while constituting the capacitor piled up on both sides of the dielectric 32 with the surface state conductors 30 and 31 like drawing 1, Power supply current flows through the surface state conductor 30 via the first terminal 30-1 of the first surface state conductor from the power supply terminal 28, and also flows into the bonding pad 26-2 for power supplies of an IC die via the second terminal 30-2 of the first surface state conductor.

[0043]Surface mounting can realize the difference with a first embodiment with the package provided with the terminal of a spherical shape while big electric capacity is obtained by forming this capacitor in the rear face of the substrate of IC die 26 and it can absorb the noise of a broadband more.

[0044]Drawing 4 is a sectional view of the ball grid array form package by a 4th embodiment of this invention. Drawing 4 is provided with the following.

Substrate 25.

The capacitor which it was allocated on this substrate 25 and formed in one end of surface state on both sides of the dielectric 32 with the first and the second surface state conductor 30 and 31 which equipped the other end of at least one the first terminal 30-1,31-1 and surface state with the at least one second terminal 30-2,31-2.

and, Two or more first signal input/output terminals 27. Two or more second signal input/output terminals 42. If small. The first power supply terminal 28 of at least one earthing terminal 29, second at least one power supply terminal 38, second at least one earthing terminal 39, third at least one power supply terminal 40, third at least one earthing terminal 41, and at least one IC die 26. The TAB package provided in the carrier film 37 is arranged in piles on a capacitor, The first power supply terminal 28 provided in the carrier film 37 is connected with the second power supply terminal 38, The second power supply terminal 38 is connected with the first terminal 30-1 of said first surface state conductor 30, It connects with the bonding pad 26-2 for power supplies of said IC die via the second terminal 30-2 of the surface state conductor 30 of this first, and the third power supply terminal 40 of the carrier film 37, The first earthing terminal 29 formed in the carrier film 37 is connected with the second earthing terminal 39, connecting the second earthing terminal 39 with the first terminal 31-1 of said second surface state conductor 31 -- this -- it connecting with the bonding pad 26-3 for grounding of said IC die 26, and via the second terminal 31-2 of the second surface state conductor 31, and the third earthing terminal 41 of the carrier film 37, It connected with the circuit pattern 35 of the carrier film 37, and the first signal input/output terminal 27 and second at least one signal input/output terminal 42 which were provided in the carrier film 37 are connected to the second signal input/output terminal 42 and the bonding pad 26-1 for signal input and output of said IC die.

[0045]Two or more first signal input/output terminals 27 and first at least one power supply terminal 28 which were provided in the carrier film 37 in drawing 4, and first at least one earthing terminal 29, Although it arranges in the shape of a lattice to a field opposite to the field which piled up this capacitor of the carrier film 37 by the spherical shape, respectively and surface mounting is made possible, pin geometry is used and it is made to perform connector mounting.

[0046]The second terminal 30-2,31-2 of the first of said capacitor and the second surface state conductor 30 and 31, It is located inside the first terminal 30-1,31-1, While the carrier film 37, the second surface state conductor 31, and the dielectric 32 are provided with the opening 43 which exposes the second terminal 30-2 of the first surface state conductor 30, the carrier film 37 is provided with the opening 44 which exposes the second terminal 31-2 of the second surface state conductor 31, Connection of connection of the third power supply terminal 40 and the second terminal 30-2 of the first surface state conductor 30, the third earthing terminal 41, and the second terminal 31-2 of the second surface state conductor 31 is enabled.

[0047]Said capacitor is printed to one field of the substrate 25 in order of the first surface state conductor 30, the dielectric 32, and the second surface state conductor 31, Forming by construction methods, such as weld slag and vacuum evaporation, the substrate 25 has the electric insulation using resin materials whose stock thickness is tens of microns - several millimeters, such as polyimide, epoxy, and phenol, and the thing of the stock thickness beyond abbreviated 1 mm has a function of the back up plate at the time of making superposition connection of the TAB package.

[0048]Since it has connected with the first earthing terminal 29, the second surface state conductor 31 and circuit pattern 35 serve as microstrip structure which countered via the carrier film 37, and the second surface state conductor 31 can extend the zone of the signal passed to the circuit pattern 35 to a high frequency region.

[0049]Drawing 5 is a sectional view of the ball grid array form package by a 5th embodiment of this invention. Drawing 5 is provided with the following.
The substrate 25 reinforced by the back up plate 45.
The capacitor which it was allocated on this substrate 25 and formed in one end of surface state on both sides of the dielectric 32 with the first and the second surface state conductor 30 and 31 which equipped the other end of at least one the first terminal 30-1,31-1 and surface state with the at least one second terminal 30-2,31-2.
and, Two or more first signal input/output terminals 27. Two or more second signal input/output terminals 42. If small. The first power supply terminal 28 of first at least one earthing terminal 29, second at least one power supply terminal 38, second at least one earthing terminal 39, third at least one power supply terminal 40, third at least one earthing terminal 41, and at least one IC die 26. The TAB package provided in the carrier film 37 is arranged in piles on a capacitor, The first power supply terminal 28 provided in the carrier film 37 is connected with the second power supply terminal 38, The second power supply terminal 38 is connected with the first terminal 30-1 of said first surface state conductor 30, It connects with the bonding pad 26-2 for power supplies of said IC die via the second terminal 30-2 of the surface state conductor 30 of this first, and the third power supply terminal 40 of the carrier film 37, The first earthing terminal 29 formed in the carrier film 37 is connected with the second earthing terminal 39, connecting the second earthing terminal 39 with the first terminal 31-1 of said second surface state conductor 31 -- this -- it connecting with the bonding pad 26-3 for grounding of said IC die 26, and via the second terminal 31-2 of the second surface state conductor 31, and the third earthing terminal 41 of the carrier film 37, The first signal input/output terminal 27 and second at least one signal input/output terminal 42 which were provided in the carrier film 37 are connected with the circuit pattern 35 of the carrier film 37, It connects with the second signal input/output terminal 42 and the bonding pad 26-1 for signal input and output of said IC die, and arranges on both sides of said capacitor with the back up plate 45 and said TAB package.
[0050]In this example, stock thickness uses for the substrate 25 the polyimide film which is an abbreviated number (10 microns - several microns), The back up plate 45 makes the substrate 25 intervene as an insulating layer using metal plates, such as aluminum and Cu, and it makes generation of heat of IC die 26 radiate heat with low thermal resistance while it prevents the electric short circuit through the back up plate 45 using the metal plate of the first terminal 31-1 of the first surface state conductor 30 and the second surface state conductor 31.
[0051]The substrate 25 may form resin materials, such as polyimide and epoxy, in the back up plate 45 by construction methods, such as a spin coat, a flow coat, and printing, and when the back up plate 45 is aluminum, an insulating layer can also be realized by an alumite treatment construction method.
[0052]In the above mentioned embodiment, although the capacitor of the layer structure which sandwiched much more dielectric layer with the surface state conductor of two sheets explained, noise absorption of a broadband is more possible by multilayer-structure-izing.
[0053]Although the example of face down bonding explained mounting of the IC die, an intention and effect of this patent are the same also in face up bonding and wire bonding.
[0054]

[Effect of the Invention]According to this invention, the advantageous effect that the noise of a broadband can be absorbed without carrying out variety a large number mounting of the capacitor of a concentrated-constant form is acquired as mentioned above.

[Brief Description of the Drawings]

【 figure 1 】 The cross section of the pin grid array form package by the first preferred embodiment of this invention

【 figure 2 】 The cross section of the pin grid array form package by the second preferred embodiment of this invention

【 figure 3 】 The cross section of the ball grid array form package by the third preferred embodiment of this invention

【 figure 4 】 The cross section of the ball grid array form package by the fourth preferred embodiment of this invention

【 figure 5 】 The cross section of the ball grid array form package which a metallic plate was used for the circuit board by the fifth preferred embodiment of this invention

【 Figure 6 】 pin grid array form ceramics package high-speed microprocessor usual

【 figure 7 】 The cross section of the semiconductor device

[Description of Notations]

25 Circuit board

26-1 Bonding pad for signal input and output

26-2 Bonding pad for the power supply

26-3 Bonding pad for connecting area

27,42 Signal input and output terminal

28,38,40 Power supply terminal

29,39,41 Earth terminal

30,31 Surface-shaped conductive body

32 Dielectric body

33 Bump

34 Overcoat

35 Wiring pattern

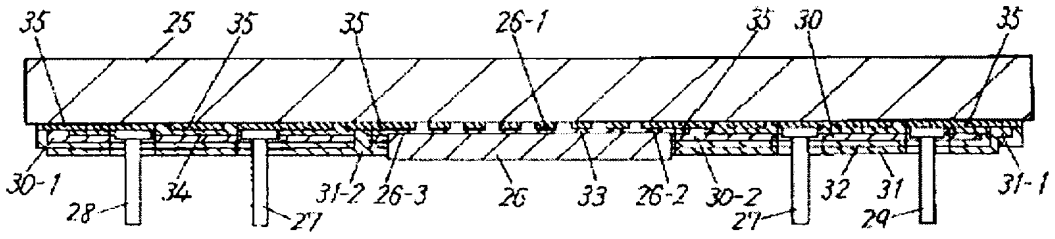
36-1,36-2,36-3,36-4,36-5 Through hole

37 Carrier film

43,44 Opening

45 Reinforcement board

【図１】



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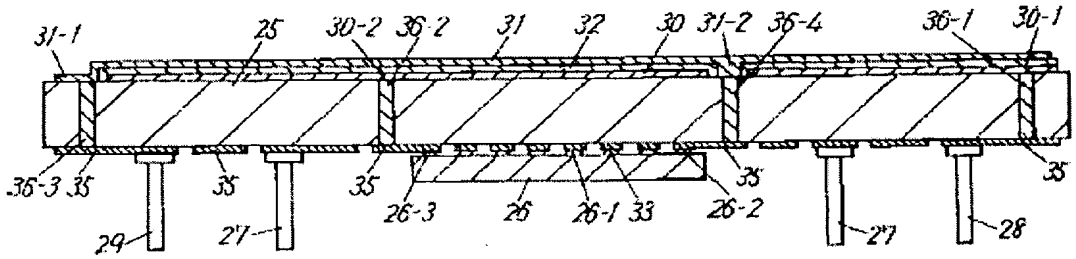
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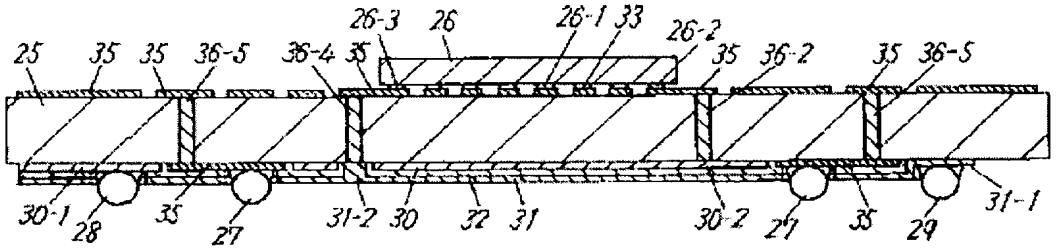
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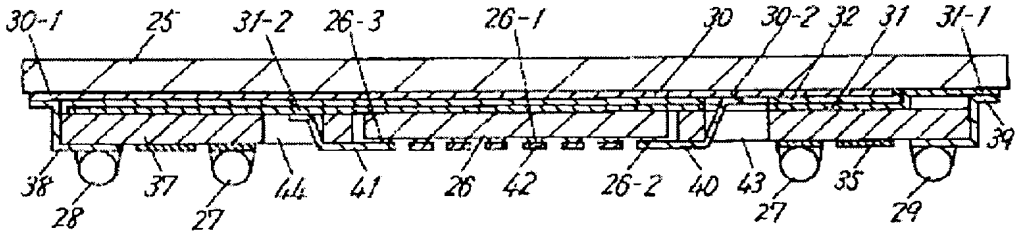
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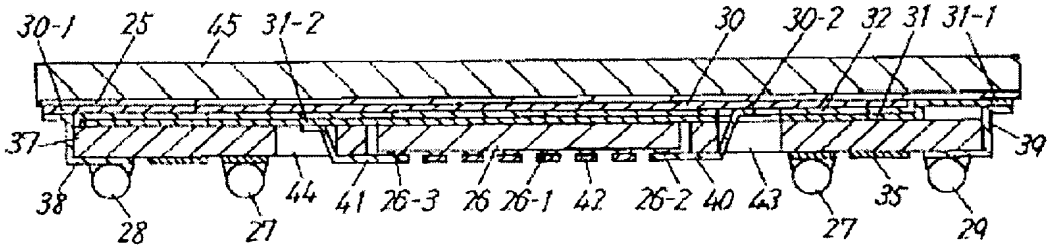
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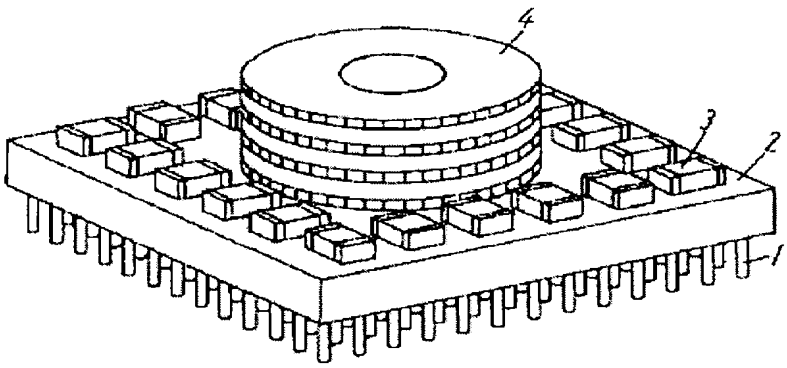

【図７】